Dr. D.Vaithiyanathan
Assistant Professor
Department of Electronics and Communication Engineering
National Institute of Technology Delhi
Sector A-7, Institutional Area, Narela, Delhi – 110040
Tele. No.: +91 1133861150
Mobile: 9865806300
Email ID : dvaithiyanathan@nitdelhi.ac.in
dvaithi@gmail.com

ACADEMIC QUALIFICATION

Degree / Diploma	University	Name of the Institution studied	Class/ Marks obtained
PhD	Anna University, Chennai	Dept. of ECE, College of Engineering Guindy	CGPA 9/10
M.E (Applied Electronics)	Anna University, Chennai	Dept. of ECE, Government College of Technology (GCT),Coimbatore	First Class With Distinction -75.48%
B.E (ECE)	University of Madras	St. Peter's Engineering College, Chennai-54.	First Class - 73.3%
Diploma (ECE)	Department of Technical Education, Chennai	Thaimoogambigai Polytechnic, Chennai	First Class with Honours - 90.9%

PhD Thesis Title: "**Low Power-Delay and High Precision Log based Floating Point Unit for Image Compression**".

WORK EXPERIENCE:

Name of the Post	Employer	Period of Employment			
		From	To	Years	Months
Assistant Professor	NIT Delhi	07.08.2017	Till date		
Teaching Fellow	College of Engineering Guindy, Anna University, Chennai	24.12.2010	04.08.2017	06	07
Lecturer	Sri Sairam Engineering College, Chennai	18.06.2009	23.12.2010	01	06
Member Technical Staff (MTS) – Chip Engineering	Digibee Microsystems Ltd., Chennai	28.06.2006	30.11.2008	02	06
Lecturer	Madha Engineering College, Chennai	05.06.2002	25.07.2004	02	02

RESEARCH INTERESTS:

Computer Architecture, VLSI Design and Embedded Systems

RESEARCH GUIDANCE:

No. of PhD Scholars Guiding – **05**
No. of M.E/M.Tech Projects Guided – **09,** Ongoing **- 05**

SUBJECTS HANDLED

Microprocessor and Micro-controller, Digital Electronics and System Design, Computer Architecture and Organization, Application Specified Integrated Circuits (ASIC) Design, Digital CMOS VLSI Design, Advanced Microprocessors and Microcontrollers, Embedded Systems, Linear Integrated Circuits, Analog and Digital Communication, Electronic Devices and Circuits.

PUBLICATIONS – INTERNATIONAL JOURNALS

1. G.Prabakaran, **D.Vaithiyanathan** and Madhavi Ganesan, **'Fuzzy Decision Support System for Improving the Crop Productivity and Efficient use of Fertilizers**', Computers and Electronics in Agriculture, Vol. 150, pp. 88-98, July 2018 (**SCIE Journal, Elsevier Publication, IF:3.171**)

2. G. Prabakaran, **D. Vaithiyanathan**, Madhavi Ganesan, "**A farmer-friendly initiative**" Grassroots, A Journal of Press Institute of India, Research Institute for Newspaper Development, August 2017

3. **Vaithiyanathan D, 'An Efficient Architecture for Carry Select Adder**', World Journal of Engineering, Vol.14, Issue: 3, pp. 249 – 254, 2017, doi: 10.1108/WJE-08-2016-0043. (**Scopus Index Emerald Publication**)

4. **J.Britto** and **D.Vaithiyanathan**, '**An Efficient Multichannel FIR Filter Architecture for FPGA and ASIC Realizations**', International Journal of Applied Engineering Research, vol. 12, no. 10, 2017, pp.2209-2220 (**Scopus Index 2010 - 2017)**

5. **D.Vaithiyanathan** and Dheepansundaravelu.P, '**Implementation of 8-Point Approximate DCT for Image Compression**', International Journal of Advanced Research in Computer Science and Software Engineering, Volume-6, Issue 9, September 2016, pp. 441-448

6. **D. Vaithiyanathan,** J. Nargis and R.Seshasayanan, '**High Performance ACS for Viterbi Decoder using Pipeline T-Algorithm**', Alexandria Engineering Journal, Vol. 54, No. 3, 2015, pp. 447-455, doi:10.1016/j.aej.2015.04.007 (**SCIE Journal, Elsevier Publication, IF:3.696**)

7. Tulasiram P. S, **D.Vaithiyanathan**, and R.Seshasayanan, '**High Speed and Area Efficient Multiplier**', Australian Journal of Basic and Applied Sciences, Volume 9, Issue-15, pp. 22-26, April 2015

8. **D. Vaithiyanathan** and R. Seshasayanan, **'An Efficient Low Power LOG Based FPU Design for FPGAs**', Advances in Natural and Applied Sciences, vol.9, no.6, 2015, pp.35-40.

9. **D. Vaithiyanathan** and R.Seshasayanan, '**Power-optimized log-based image processing system**', *EURASIP Journal on Image and Video Processing*, 2014:37, pp. 1-15,doi: 10.1186/1687-5281-2014-37 (**SCIE Springer Publication, IF: 1.534**)

10. **D. Vaithiyanathan**, R. Seshasayanan, K. Kunaraj, and J. Keerthiga, '**An Evolved Wavelet Library Based on Genetic Algorithm**', The Scientific World Journal, vol. 2014, Article ID 494319, 17 pages, 2014. doi:10.1155/2014/494319 **(Scopus Index Hindawi Publication)**

11. **D. Vaithiyanathan** and R.Seshasayanan, '**Area and Power Efficient DCT Architecture for Image Compression**', *EURASIP Journal on Advances in Signal Processing*, **2014**:180, pp. 1-9, doi: 10.1186/1687-6180-2014-180 (**SCIE Springer Publication, IF: 1.749**)

12. Tulasiram P. S, **D.Vaithiyanathan**, and R.Seshasayanan, '**Implementation of Modified Booth Recoded Wallace Tree Multiplier for Fast Arithmetic Circuits**', International Journal of Advanced Research in Computer Science and Software Engineering, Volume-4, Issue-10, pp. 798- 802, October 2014.

13. **D.Vaithiyanathan**, K.Kunaraj, S.Anith and R.Seshasayanan, '**Multiplierless 8-Point DCT Architecture for Fast Image Compression**', International Journal of Applied Engineering Research, vol. 9, no. 20, 2014, pp.4533-4538 (**Scopus Index 2010 - 2017)**

PUBLICATIONS – INTERNATIONAL CONFERENCES

1. J.Britto Pari and **D.Vaithiyanathan,** "**An Optimized FPGA Implementation of DCT Architecture for Image and Video Processing Applications**", Proc. International Conference on Wireless Communications Signal Processing and Networking, Chennai, India, March 21-23, 2019
2. **D.Vaithiyanathan**, J.Britto Pari, S.Keerthana and Kala Bharathan, "**Implementation of Floating Point Unit based on Booth Multiplier and Compressor Adder**", Proc. International Conference on Electrical, Computer and Communication Technologies, Coimbatore, India, Feb. 20-22, 2019.
3. M Bharathi Raj, S Ewins Pon Pushpa and **D.Vaithiyanathan**, "**Investigation of Negative capacitance - MoS2 based nanotube transistor sandwiched with polyvinylidence fluoride as ferroelectric gating material**", Proc. International Workshop on Nano/Micro 2D-3D Fabrication, Manufacturing of Electronic - Biomedical Devices & Applications at Indian Institute of Technology(IIT), Mandi, India, Oct. 31 - Nov. 02, 2018
4. M Bharathi Raj, S Ewins Pon Pushpa and **D.Vaithiyanathan**, "**Performance Analysis of 7-nm node Negative capacitance - MoS2 nanotube transistor based SRAM**", Proc. International Workshop on Nano/Micro 2D-3D Fabrication, Manufacturing of Electronic - Biomedical Devices & Applications at Indian Institute of Technology(IIT), Mandi, India, Oct. 31 - Nov. 02, 2018
5. **D.Vaithiyanathan,** M Bharathi Raj, S Ewins Pon Pushpa and R.Seetharaman, **"Performance analysis of FinFET and Negative Capacitance FET over 6T SRAM"**, Proc. IEEE International Conference on Circuits and Systems (ICCS 2017), Thiruvananthapuram, India, pp. 196 - 200, Dec. 20-21,2017
6. L.Sakthivel, **D.Vaithiyanathan** and R.Seshasayanan, "**Realization of Conventional Measuring Instruments using FPGA**", Proc. International Conference on Recent Trends and Advancement In Information and Communication Engineering, Coimbatore, India, 2015
7. R.D. Janani, **D.Vaithiyanathan** and R.Seshasayanan, "**Inverter Based Two Stage CMOS Differential Amplifier**", in Proceeding of the International Conference on IntelligentEngineering Systems, Coimbatore, India, April 3 – 4, 2014.
8. **D.Vaithiyanathan** and R.Seshasayanan, "**High speed low power DWT structure with log based FPU in FPGAs**", in Proceeding of the International conference on Green Computing,Communication and Conservation of Energy (ICGCE 2013), Chennai, pp. 308 – 313, India Dec. 12 – 14, 2013. doi: 10.1109/ICGCE.2013.6823451
9. **D.Vaithiyanathan**, R.Seshasayanan, S.Anith and K.Kunaraj "**A low-complexity DCT approximation for image compression with 14 additions only**", in Proc. of theInt. conference on Green Computing, Communication and Conservation of Energy (ICGCE 2013), Chennai, pp.303–307, Dec. 12 – 14, 2013. doi: 10.1109/ICGCE.2013.6823450
10. **D.Vaithiyanathan** & R. Seshasayanan,"**Low power DCT architecture for imagecompression**", in Proceeding of the International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, pp.1-6, Dec. 19-21, 2013 doi: 10.1109/ICACCS.2013.6938745
11. K.Sathish Raj, **D.Vaithiyanathan** and P.Sakthivel, "**Design of Pixel Based CMOS ImageSensor Device**",Proc. International conference on Communication and Signal Processing– **ICCSP – 2013",** pp. 1155–1158, April 3-5, 2013. doi: 10.1109/iccsp.2013.6577237
12. S.Mahendran, **D.Vaithiyanathan** and R.Seshasayanan, "**Object Tracking System Based onInvariant Features**", Proc. International conference on Communication and SignalProcessing – **ICCSP– 2013",** pp. 1138 – 1142, April 3-5, 2013. doi: 10.1109/iccsp.2013.6577234
13. K.Saraswathy, **D.Vaithiyanathan** and R.Seshasayanan, "**A DCT Approximation with LowComplexity for Image Compression**", Proc. International conference on Communicationand Signal Processing – **ICCSP– 2013",** pp. 465 – 468, April 3-5, 2013. doi: 10.1109/iccsp.2013.6577097
14. D.Karthikeyan, **D.Vaithiyanathan** and R.Seshasayanan, "**Guaranteed throughput innetwork on-chip using alternate path switch**", Proc. International Conference on FuturisticTrends in Electronics Engineering – **ICFTEE– 2013",** Vol. 4, 2nd& 3rd March 2013.

15. G.Bharathi and**D.Vaithiyanathan**, "**Adaptive Pixel Pair Matching for a Novel DataEmbedding**", Proc. International Conference on Futuristic Trends in Electronics Engineering– **ICFTEE– 2013",** Vol. 4, 2nd& 3rd March 2013.
16. S.Anith, **D.Vaithiyanathan** and R.Seshasayanan, "**Face Recognition System Based onFeature Extraction**", Proc. International Conference on Information Communication andEmbedded Systems – **ICICES 2013**, pp. 646 – 651, Feb 2013. doi: 10.1109/ICICES.2013.6508266
17. J.Nargis, **D.Vaithiyanathan** and R.Seshasayanan, "**Design of High Speed Low PowerViterbi Decoder for TCM System**", Proc. International Conference on InformationCommunication and Embedded Systems – **ICICES 2013**, pp. 185 – 190, Feb 2013. doi:10.1109/ICICES.2013.6508239
18. Harish Anand .T, **D.Vaithiyanathan** and R.Seshasayanan "**Optimized Architecture forFloating Point Computation Unit**", Proc. International Conference on Emerging Trends inVLSI, Embedded Systems, Nano Electronics & Telecommunication Systems – **ICEVENT2013**, pp. 1–5, Jan 2013. doi: 10.1109/ICEVENT.2013.6496587
19. **D.Vaithiyanathan**, R .Satyabama andR.Baskaran "**An Escalated Architecture for Spline Based Biorthogonal Wavelet Transforms and their Application in Image Compression**",Proc. International Conference on Innovative Computing, Information and Communication Technology – **ICICT'09**, Dec 2009.

PUBLICATIONS – NATIONAL CONFERENCES

1. Bagyaraj S, Ragumathulla M and **D.Vaithiyanathan**, "**Acquisition of Jugular Venous Pulse Waveform by a Non Invasive Technique**" Proc. IST National Conference on Advances In Mechanical Engineering-2019 (NCAME-2019), National Institute of Technology, Delhi, India, 16, March 2019.
2. Suruchi Sharma, Santosh Kumar, Alok Kumar Mishra, **D. Vaithiyanathan** and Baljit Kaur, "**PVT Aware Analysis of ISCAS C17 Benchmark Circuit**" Proc. IST National Conference on Advances In Mechanical Engineering-2019 (NCAME-2019), National Institute of Technology, Delhi, India, 16, March 2019.
3. L.Suletha and **D.Vaithiyanathan, "**Hardware Optimized DCT Implementation using Adders Only**"** Proc. National Conference on Instrumentation, Electrical and Electronics Engineering (NCIEEE'16), Saveetha Engineering College, Thandalam, Chennai, India, 1st April 2016.
4. R.Ramya and **D.Vaithiyanathan, "Implementation of Elliptic Curve Cryptosystem using Redundant Basis Multiplier"** Proc. National Conference on Instrumentation, Electrical and Electronics Engineering (NCIEEE'16), Saveetha Engineering College, Thandalam, Chennai, India, 1st April 2016.
5. M.S.Vinotheni and **D.Vaithiyanathan, "FIR Filter Implementation using MLCP Booth Multiplier of S-BP Recording Techniques"** Proc. National Conference on Instrumentation, Electrical and Electronics Engineering (NCIEEE'16), Saveetha Engineering College, Thandalam, Chennai, India, 1st April 2016.
6. K.Bhuvana, **D.Vaithiyanathan** and R.Seshasayanan, "**Efficient Architecture of AES by using Composite S-Box and Mix Coloumn Transformation**" Proc. National Conference on Integrated Circuits, EGS Pillay Engineering College, Nagapattinam, India, 2015
7. Dheepansundravelu P, **D.Vaithiyanathan** and R.Seshasayanan, "**8-Point Approximate DCT for Image Compression**", Proc. 7th National Conference on Signal Processing, Communication and VLSI Design (NCSCV `15), Anna University Regional Centre, Coimbatore, India, 2015
8. T.Duraimurugan, **D.Vaithiyanathan** and R.Seshasayanan, "**An Efficient 4-Parallel FFT Architecture**", Proc. National Conference on Recent Enhancement in Advanced Computing Technologies (NC-REACT `14)", Rrase College of Engineering, Chennai India, 2014
9. H.Harini, **D.Vaithiyanathan** and R.Seshasayanan, "**Turbo Decoders for LTE**", Proc. National Conference on Innovative Electronics & Wide Range Technologies **- NCIEWT `14**", Sri Krishna Engineering College, Chennai, India, 2014
10. S.Ramya, **D.Vaithiyanathan** and R.Seshasayanan, "**A New Channel Estimation method for STBC-OFDM Downlink Baseband Receiver for Mobile WMAM**", Proc. National Conference on Magus Info Electro Tech – 14 **MIET `14**", Madha Institute of Engineering and Technology, Chennai, India, 2014

11. T.Duraimurugan, **D.Vaithiyanathan** and R.Seshasayanan, "**An Efficient 4-Parallel Feed Forward FFT Architecture**", Proc. National Conference on Magus Info Electro Tech – 14,Madha Institute of Engineering and Technology, Chennai, India, 2014
12. R.Sasikala, **D.Vaithiyanathan** and R.Seshasayanan, "**Logarithmic Number System and their impact on FIR Filter**", Proc. 1st National Conference on Recent Trends in Electronics and Communication – **RTEC`13**", St.Joseph College of Engineering, Chennai, India, April 2013, pp. 22 – 26
13. P.Surya, **D.Vaithiyanathan** and R.Seshasayanan, "**Design of Low Power and Area Efficient Parallel Pipelined FFT Architecture**", Proc. National Conference on Recent Trends in Electrical and Communication Engineering – **NCRTECE`13**", 2013
14. **D.Vaithiyanathan**, Prof. R .Satyabama, Dr.S.Annadurai, "**Design of Biorthogonal Wavelets using Linear Phase Filter in Lifting Scheme**", Proc. National Conference on Issues and Trends in Advanced Computing – **NITAC'06**, pp. 64, May 2006
15. **D.Vaithiyanathan**, R.Satyabama, S.Annadurai, "**Construction of Spline Based Biorthogonal Wavelet Transforms and their Application in Image Compression**",Proc. National Conference on Communication Technologies – **NCCT'06,**pp. 197–201, March 2006

CONFERENCES/SEMINAR/WORKSHOPS – CONDUCTED

Sl. No.	From	To	Name of Courses	Place
1.	16.03.2019	--	National Conference on Advances in Mechanical Engineering-2019 (NCAME-2019)	National Institute of Technology, Delhi
2.	18.12.2017	22.12.2017	Hands-on Session on VLSI Design Tools	Dept. of ECE, National Institute of Technology, Delhi.
3.	08.11.2017	08.11.2017	Workshop on Semiconductor Process and Device Simulations	Dept. of ECE, National Institute of Technology, Delhi.
4.	23.07.2013	27.07.2013	Faculty Development Training Programme on VLSI Design for TEQIP – II Institutions	The Checkers Hotel, Chennai
5.	05.12.2012	11.12.2012	Faculty Development Training Programme on EC254 VLSI Design	Dept. of ECE, CEG, Anna University, Chennai – 600 025
6.	07.10.2010	08.10.2010	Workshop on VLSI Design Methodology & Tools	Dept. of ECE, Sri Sairam Engg. College, Chennai - 44

PG Dissertation Guided

Sr. No.	Title of Dissertation / Project	Year	Name of student	Co-Supervisor(s), if any
1	Design and Analysis of Pulse Triggered D Flip-Flop	May 2019	Richa Thakur	NA
2	Design and Implementation of Non-Volatile Memory Low Power Multi-Scaling Voltage Level Shifter	May 2019	Megha Singh Kurmi	NA
3	Design and Analysis of Low Power and High Read Stability 7T SRAM Cell	May 2019	Yogesh Pal	NA
4	Power Reduction of DET Flip-Flop using Lector Technique	May 2019	Vikrant Gupta	NA
5	Performance Analysis of Dynamic CMOS Circuit based on Node-Discharge and Twisted-Connected Transistor	May 2018	Ravindra Kumar	NA
6	Design and Implementation of Compressor Adder with Modified Booth Based Floating Point Multiplier	May 2017	Keerthana S	NA
7	Implementation of Elliptic Curve Cryptosystem using Redundant Basis Multiplication	May 2016	Ramya R	NA

8	FIR Filter Implementation using MLCP Modified Booth Multiplier with BIT Pairing Techniques	May 2016	Vinotheni M S	NA
9	Hardware Optimized DCT Implementation	May 2016	Suletha L	NA

UG Dissertation Guided

Sr. No.	Title of Dissertation / Project	Year	Name of student	Co-Supervisor(s), if any
1	Automated Vehicle Driving System using OPENCV	April 2019	Nisha Tanuj Kumar	NA
2	Conception and Realization of a 3D Printer	April 2019	Pedada Venkata Tejaswi Soumesh Dehury	NA
3	Underwater Wireless Optical Communication using LED/LASER	April 2019	G.Rajapraneeth Reddy K.Sanjeeva Narayana	NA
4	IoT Based Smart City	April 2019	Burrisrujana Dokala Poornima	NA
5	Railway Track Crack Detection	April 2019	Vinod Dabriya Prabhat Kumar Satya	NA
6	Smart Irrigation System Using IoT	April 2018	Parsa Surya Teja	NA
7	Human Detection Robot Using Passive Infrared Sensor	April 2018	Paloju Vasudev Poojitha Chegireddy	NA
8	Home Automation Using IoT	April 2018	Varsha Ghanghor	NA
9	WEHICLE - A Web Controller Vehicle	April 2018	Abhijeet Mohapatra	NA
10	Arduino based Shadow Alarm for Security	April 2018	Vaditya Ranapratap	NA
11	Jewellery Shop Security System at Night Time by Using Ultrasonic Sensor	April 2017	Manonmani V Elumalai K Ramakanth S Satya K	NA
12	Wireless Gesture Controlled Robot	April 2015	Vigneshwaran V Divya V Deepika R, Gayathri K	NA
13	Analysis of CT Liver Images for Tumor Diagnosis based on Supervised Classifier and Clustering Model	April 2015	Thenkavi E Kaviya B Manoranjitha A Sriram	NA
14	Recognition of Hand-Drawn Circuits	April 2015	Poorani B Regha S Elakkiya B Archana R	NA
15	Prepaid Energy Meter with GSM Technology	April 2014	Abimanyu Arora Nimesh A Padmanabha CV Paveethraa S	NA
16	Design of RF Coupling & Decoupling Network	May 2013	Ambalavanan S Narendiran T Ravikumar K Senthil Kumar R	NA
17	Implementation of Arithmetic Coder in FPGA	May 2013	Saravanan K Sathiss Ananth MV Siddarth R	NA
18	Fractal Image Compression Using Quadtree Decomposition	May 2013	Vignesh M Vikash M Vikraman K Vinoth V	NA

INVITED LECTURES

1. Delivered a Lecture on "VLSI Design" organized by Velammal Institute of Technology, Thiruvallur-601204 (23-February-2019)
2. Delivered a Lecture on "Recent Trends in VLSI Design" organized by Vel Tech Engineering College, Chennai-600062 (22-February-2019)
3. Delivered a Lecture on "Full Custom, Semi Custom and FPGA building blocks" in Faculty Development Programme on "EC6601 - VLSI Design" organized by College of Engineering Guindy, Anna University, Chennai (22nd & 23rd-November-2018)
4. Delivered a Lecture on "VLSI Design - Design of Arithmetic Circuits" organized by Galgotias College of Engineering and Technology, Greater Noida - 201306 (13-November-2018)
5. Delivered a Lecture on "Digital circuit implementation on FPGA" organized by ABES Engineering College, Ghaziabad, U.P.-201009 (29-September-2018)
6. Delivered a Lecture on "8051 Microcontroller and its Interfacing" organized by Velammal Engineering College, Chennai-600066 (24-August-2018)
7. Delivered a Lecture on " Microprocessor and Microcontroller" in Faculty Development Training Programme organized by College of Engineering Guindy, Anna University, Chennai (31-May-2018 & 01-June-2018)
8. Delivered a Lecture on "Microprocessor & Microcontroller" and "Embedded Systems" organized by R.M.K. Engineering College, Kavaraipettai - 601206 (29-December-2017)
9. Delivered a Lecture on "VLSI Design Techniques" in two days Faculty Development Programme on VLSI Advanced Design Techniques using Tanner Tool organized by Hindustan University, Chennai-603103 (08-June-2017)
10. Delivered a Lecture on "VLSI Design" organized by Vel Tech Engineering College, Chennai-600062 (10-March-2017)
11. Delivered a Lecture on "VLSI Design" organized by Madha Engineering College, Chennai-600069 (09-April-2016)
12. Delivered a Lecture on "VLSI Design" organized by Velammal Engineering College, Chennai-600066 (12-March-2016)
13. Delivered a Lecture on "EC6504-Microprocessor and Microcontroller" in Faculty Development Training Programme organized by Jaya Engineering College, Chennai – 602024 (09-May-2015)
14. Delivered a Lecture on "Microprocessor - Memory and I/O Interfacing" organized by Loyola- ICAM College of Engineering and Technology, Chennai - 600034 (21-March-2012)

FDP/Workshops/Seminars – Attended

Sl. No.	From	To	Name of Courses	Place
1.	17.12.2018	22.12.2018	AICTE Sponsored Short Term Course on Phase-Locked Loops	IIT Madras, Chennai - 600036
2.	29.01.2018	02.02.2018	Instructional Enhancement Program on Analog IC Design	IIT Madras, Chennai - 600036
3.	19.06.2017	25.06.2017	FDP on Digital Image Processing	SSN College of Engineering, Chennai
4.	22.05.2017	28.05.2017	FDP on Advanced Computer Architecture	Anna University, Chennai – 600 025
5.	15.05.2017	21.05.2017	FDP on Computer Architecture	MIT Campus, Anna University, Chennai – 600 044
6.	12.05.2017	----	Scope for R&D Projects and Proposal Preparation	Anna University, Chennai – 600 025

7.	10.03.2017	11.03.2017	Field Programmable Analog Array	Anna University, Chennai – 600 025
8.	27.02.2017	----	Springer Nature Author Workshop	Anna University, Chennai – 600 025
9.	03.08.2016	----	Routledge Editorial Workshop 2016	Anna University, Chennai – 600 025
10.	05.05.2016	11.05.2016	FDP on Microprocessor and Microcontroller	Anna University, Chennai – 600 025
11.	02.11.2015	----	Author workshop	Anna University, Chennai – 600 025
12.	29.10.2015	30.10.2015	Advancements in Biomedical Signal and Image Processing	MIT Campus, Anna University, Chennai – 600 044
13.	22.09.2015	---	Regional Training Programme on URKUND – An Anti Plagiarism Detection Tool	Anna University, Chennai – 600 025
14.	09.07.2015	13.07.2015	Foundation Skills in Integrated Product Development (FSIPD) Train-the-Trainer Program	Anna University, Chennai – 600 025
15.	23.03.2015	24.03.2015	WBAN-Sensing and Signal Processing Challenges	Anna University, Chennai – 600 025
16.	12.03.2015	14.03.2015	Digital Custom IC Design using CADENCE EDA Tools	Anna University, Chennai – 600 025
17.	08.12.2014	14.12.2014	FDP on Principles of Digital Signal Processing	Anna University, Chennai – 600 025
18.	23.11.2013	24.11.2013	Lecturer on “How to do a good PhD Thesis”	Anna University, Chennai – 600 025
19.	28.06.2013	---	R&D Project Proposals – Awareness, Needs and Benefits	Anna University, Chennai – 600 025
20.	12.04.2013	13.04.2013	Two day workshop on end-to-end exploration of MATLAB for image analysis	Anna University, Chennai – 600 025
21.	04.04.2013	05.04.2013	Two day workshop on Agilent ADS (Adv. RF Design S/W)	Anna University, Chennai – 600 025
22.	22.03.2013	23.03.2013	WBAN – Challenges and Enabling Technologies	Anna University, Chennai – 600 025
23.	08.03.2013	09.03.2013	Research Methodology, Techniques of writing Research Articles for SCI Journals and PhD Thesis preparation	Anna University, Chennai – 600 025
24.	29.01.2013	---	How to write for and get published in scientific journals and publish manuscripts	Anna University, Chennai – 600 025
25.	10.01.2013	---	One day workshop on micro-electromechanical systems	Anna University, Chennai – 600 025
26.	19.12.2012	---	Workshop on national e-Governance plan	MIT,Anna University, Chennai – 600 044
27.	15.10.2012	16.10.2012	Two days workshop on Image processing framework using FPGA	MIT,Anna University, Chennai – 600 044
28.	05.10.2012	06.10.2012	Two day hands-on workshop on Semiconductor solutions for wireless communication	Anna University, Chennai – 600 025
29.	28.03.2012	29.03.2012	Two days workshop on Video Analytics	MIT,Anna University, Chennai – 600 044
30.	27.09.2012	---	One day workshop on Renesas 16 bit RL78 Microcontrollers	Anna University, Chennai – 600 025
31.	14.09.2012	15.09.2012	Two days seminar on Analog IC Design	MIT,Anna University, Chennai – 600 044
32.	27.07.2012	28.07.2012	Hands on session on network security	Anna University, Chennai – 600 025
33.	30.06.2012	--	Sir C.V. Raman Lecturer on Research Paper Publications in Journals	IET Chennai Network, Hotel Benz Park, Chennai
34.	14.06.2012	16.06.2012	4th Training/Workshop on planning and preparing a	CLRI, Adayar,

			best PhD thesis of an international quality	Chennai – 600 020
35.	21.05.2012	27.05.2012	FDP on IT2401 – Service oriented architecture	Anna University, Chennai – 600 025
36.	07.05.2012	13.05.2012	FDP 0n CS2301-Software Engineering	Anna University, Chennai – 600 025
37.	03.05.2012	---	Adding WiFi capability to microcontroller based sensor and control applications	Anna University, Chennai – 600 025
38.	11.04.2012	12.04.2012	Evolutionary Issues in Software Engineering	Anna University, Chennai – 600 025
39.	31.01.2012	---	One day workshop on Renesas 16 bit RL78 Micrcontroller	Anna University, Chennai – 600 025
40.	16.12.2011	17.12.2011	Design optimization using Xilinx planahead & partial reconfiguration	Oxford Engineering College, Trichirappalli - 09
41.	17.11.2011	19.11.2011	FDP on Advanced VLSI design	SSN College of Engineering, Chennai
42.	23.08.2011	---	Essential of FPGA Design conducted during Xilinx Technical knowledge summit 2011- 2012	Chennai, India
43.	19.04.2011	20.04.2011	Low power embedded systems using MSP430 microcontroller	Anna University, Chennai – 600 025
44.	15.11.2010	18.11.2010	EDA tools for VLSI Design and Signal Processing	SSN College of Engineering, Kalavakkam
45.	01.05.2010	02.05.2010	Two day workshop on Low Power Embedded System using MSP430 Microcontroller	BMS college of Engineering, Bangalore.
46.	06.03.2010	---	FDP on VHDL Programming	Sri Sai Ram Engg College, Chennai
47.	16.12.2009	18.12.2009	Tutorial session on Wireless Sensor Networks	Sri Sai Ram Engg College, Chennai